REMARKS

Claims 1-8, 17-22, and 34-41 were pending in the present application. In the above amendments, claims 1-8, 17-19, 21-22, 33-34, and 36-41 have been amended, and new claims 42-45 have been added. Therefore, after entry of the above amendments, claims 1-8, 17-22, and 34-45 will be pending in this application. Applicant believes that the present application is now in condition for allowance, which prompt and favorable action is respectfully requested.

Rejection of Claims 1-8, 17-22, and 34-41 Under 35 U.S.C. §102(b)

Claims 1-8, 17-22, and 34-41 stand rejected under 35 U.S.C. §102(b) as being anticipated by Welland (U.S. Patent No. 6,137,372).

Welland describes a frequency synthesizer/phase-locked loop (PLL) **500** having a voltage controlled oscillator (VCO) **400**. VCO **400** has discretely variable capacitance that provides coarse tuning adjustment and continuously variable capacitance that provides fine tuning adjustment. (See the Abstract.)

When PLL **500** initiates, control of the output frequency **102** lies with discrete control block **502**. Discrete control block **502** determines how to adjust the discretely variable capacitance to coarsely tune the output frequency **102**. Discrete control block **502** may adjust the digital control word **404** used to provide control signals to the discretely variable capacitance **404** within VCO **400**. (See column 9, lines 12-33.)

Once the discrete control block **502** completes its coarse tuning procedure, the discrete control block **502** asserts the START signal **506** to change switch **512** so that it deselects the control mode **510**. At this point, counters **204** and **214** are reset with the zero-phase restart (ZPR) signal **505**. The zero-phase restart (ZPR) signal **505** presets counters **204** and **214** so that the initial phase error is as small as possible when the first analog loop becomes operational." (See column 9, lines 34-46.)

Claim 1 of the present invention, as amended, recites:

> "A method of calibrating an oscillator comprising:
> generating a first signal indicative of a frequency of the oscillator;

generating a second signal indicative of a reference frequency, wherein the generating the first and second signals comprises scaling the frequency of the oscillator and scaling the reference frequency at approximately the same time so that the first and second signals are substantially in phase for calibration of the oscillator; and

adjusting the frequency of the oscillator based on a comparison of the first and second signals."

Applicant submits that claim 1 is not anticipated by Welland for at least the following reason. Welland does not describe "scaling the frequency of the oscillator and scaling the reference frequency at approximately the same time so that the first and second signals are substantially in phase for calibration of the oscillator," as claim 1 recites. As noted above, Welland resets the zero-phase restart (ZPR) signal **505** after the coarse tuning procedure is completed so that the initial phase error is as small as possible when the first analog loop becomes operational. This feature of Welland is similar to the feature of new claim 43 of the present application. However, Welland does not generate signals **216** and **218** to be inphase during coarse tuning or calibration of the oscillator. Hence, Applicant submits that claim 1 is not anticipated by Welland.

Claims 2-8 are dependent on claim 1 and are not anticipated by Welland for at least the reason noted for base claim 1. These dependent claims may recite additional features not disclosed by Welland.

For claim 3, Welland does not describe "generating a calibration voltage based on temperature" and "applying the calibration voltage to the oscillator for calibration of the oscillator." The rejection states that this feature is disclosed by Welland in column 7, line 65 to column 8, line 25. However, this section states "after the initial calibration, the continuously variable capacitance **406** may be used to compensate for any post-calibration frequency drift", which may be due to a variety of factors including temperature variations. Welland thus relies on the continuously variable capacitance **406** to account for frequency variations due to temperature after calibration has been performed. Welland does not generates a calibration voltage based on temperature that is used for calibration of the oscillator, as claim 3 recites.

For claim 4, Welland does not describe "testing a voltage control input to the oscillator from the phase locked loop to determine whether calibration should be performed again." The

rejection states that this feature is disclosed by Welland in column 9, lines 11-33. However, this section simply describes the coarse tuning procedure, which is summarized above. This section does not describe the possibility of performing coarse tuning at a future time and hence does not describe testing a voltage control input to determine whether calibration should be performed again.

For claim 5, Welland does not describe "receiving the reference frequency from a temperature compensated crystal oscillator." Welland describes using a reference frequency **106** from a crystal oscillator **105**. However, Welland does not describe using a temperature compensated crystal oscillator, which may provide better frequency accuracy over different temperatures and is desirable for certain applications such as, e.g., wireless communication.

For claim 8, Welland does not describe "adjusting a gain of a charge pump of the phase lock loop based on a calibration setting of the oscillator." The rejection states that this feature is disclosed by Welland in column 8, line 58 to column 9, line 5. However, this section simply describes the operation of an ordinary PLL. Different calibration settings may result in different gains Kv for the oscillator, which may result in different loop characteristics for the PLL. The gain of the charge pump may be adjusted to compensate for the different gains Kv, so that (1) the total gain is approximately constant and (2) the PLL loop characteristics do not change for different calibration settings. This feature of claim 8 is described in paragraphs [0054] and [0055] of the present application. Welland does not describe this feature of claim 8.

Claims 17, 18, 19, 20, 21 and 22 recite features similar to the features of claims 1, 2, 3, 5, 6 and 7, respectively. Claims 17, 18, 19, 20, 21 and 22 are not anticipated by Welland for the reasons noted above for claims 1, 2, 3, 5, 6 and 7.

For independent claim 34, Welland does not describe "selecting a calibration voltage for an oscillator based on temperature" and "calibrating the oscillator based on a frequency of the oscillator with the calibration voltage applied." As noted above for claim 3, Welland does not perform coarse tuning to account for temperature. Rather, Welland relies on the continuously variable capacitance **406** to account for frequency variations due to temperature after calibration has been performed. Hence, claim 34 is not anticipated by Welland.

Claims 35-37 are dependent on claim 34 and are not anticipated by Welland for at least the reason noted for base claim 34. For claim 36, Welland does not describe "selecting a

calibration voltage based on a proportional to absolute temperature (PTAT) voltage." This feature is described in paragraph [0033].

Claims 38-41 recite features similar to the features of claims 34-37, respectively. Claims 38-41 are not anticipated by Welland for the reasons noted above for claims 34-37.

Accordingly, the §102(b) rejection of claims 1-8, 17-22, and 34-41 should be withdrawn.

New Claims

New claims 42-45 recited additional features of the invention. Claims 42-44 are dependent on claim 1 and are not anticipated by Welland for at least the reason noted above for base claim 1. Claim 45 is dependent on claim 34 and is not anticipated by Welland for at least the reason noted above for base claim 34.

CONCLUSION

In light of the amendments contained herein, Applicant submits that the application is in condition for allowance, for which early action is requested.

Please charge any fees or overpayments that may be due with this response to Deposit Account No. 17-0026.

Respectfully submitted,

Dated: 11/9/05

By: _____
George C. Pappas, Reg. No. 35,065
858-651-1306

QUALCOMM Incorporated
Attn: Patent Department
5775 Morehouse Drive
San Diego, California 92121-1714
Telephone: (858) 658-5787
Facsimile: (858) 658-2502